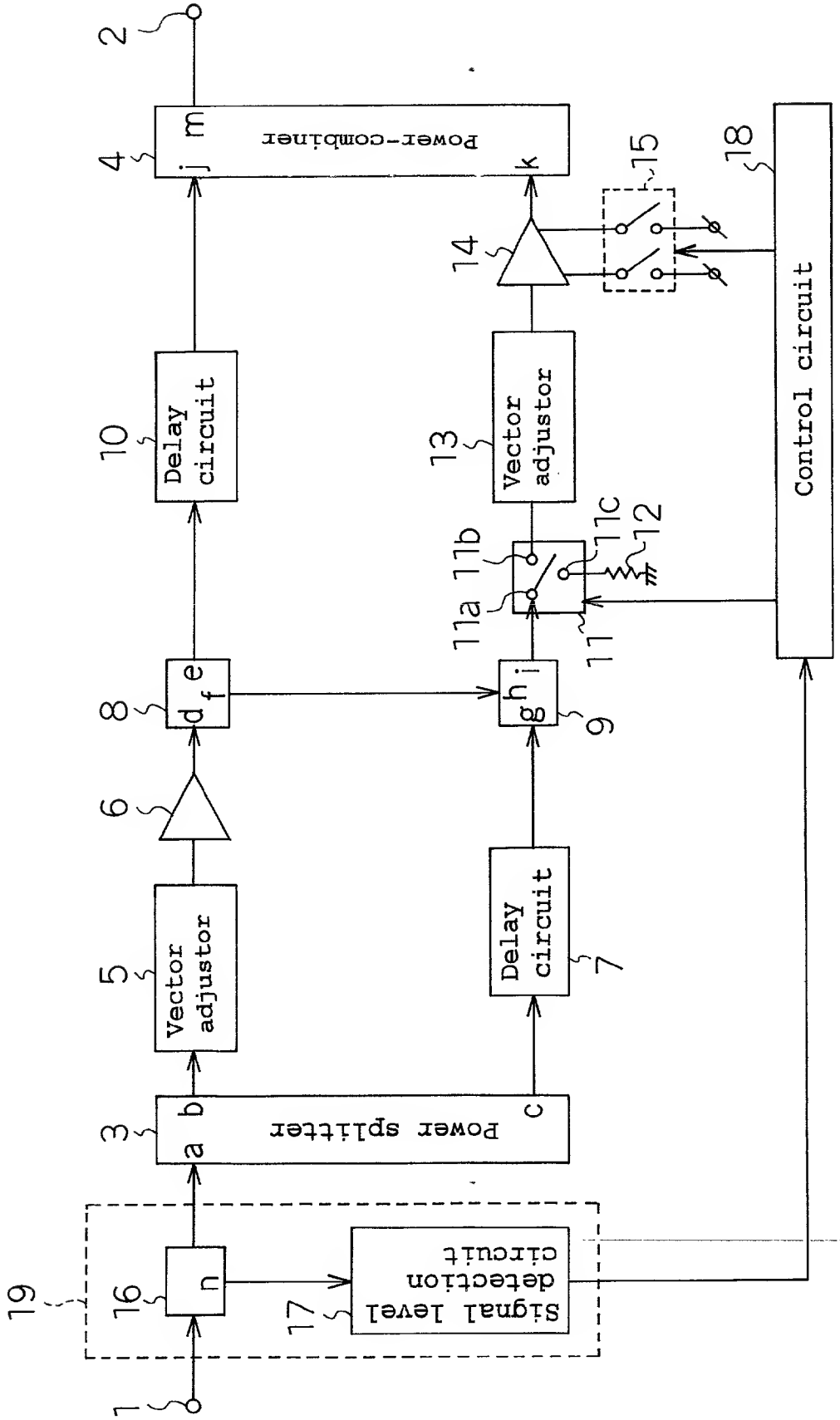

1
2
3
Power splitter
a
b
c
4
Power-combiner
j
m
k
5
Vector adjustor
6
7
Delay circuit
8
d
e
f
9
g
h
i
10
Delay circuit
11
11a
11b
11c
12
13
Vector adjustor
14
15
16
n
17
Signal level detection circuit
18
Control circuit
19

Fig. 1

847 Fig. 2 3

Fig. 2

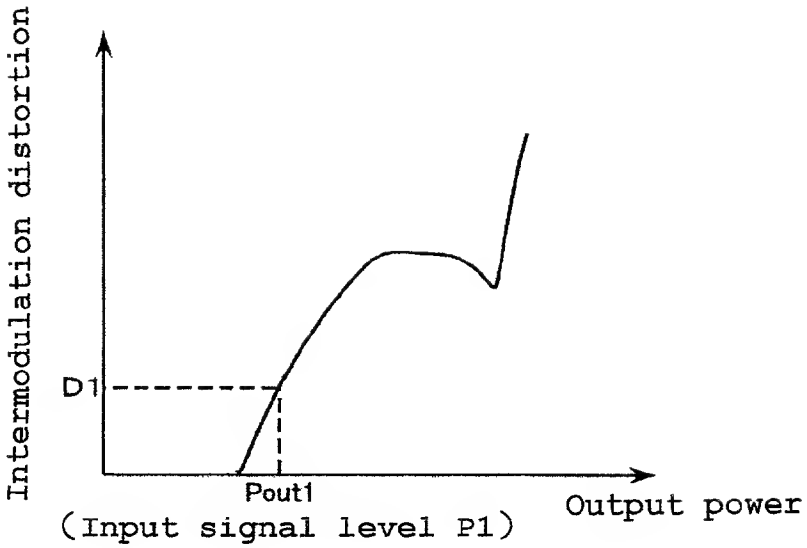
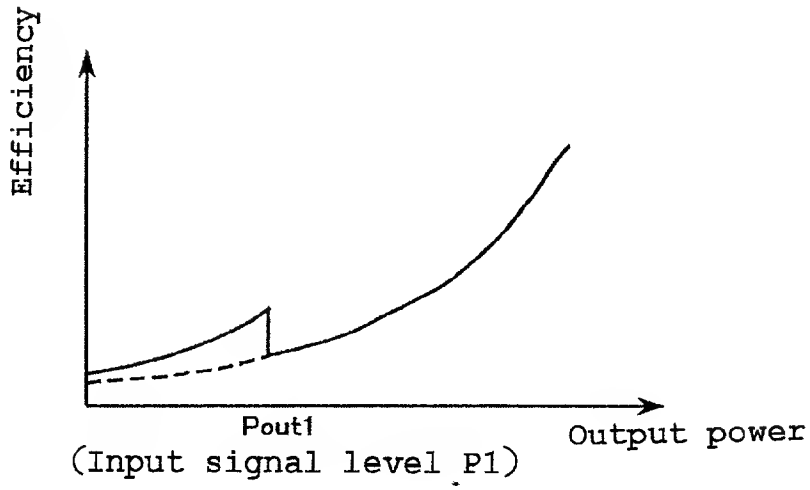
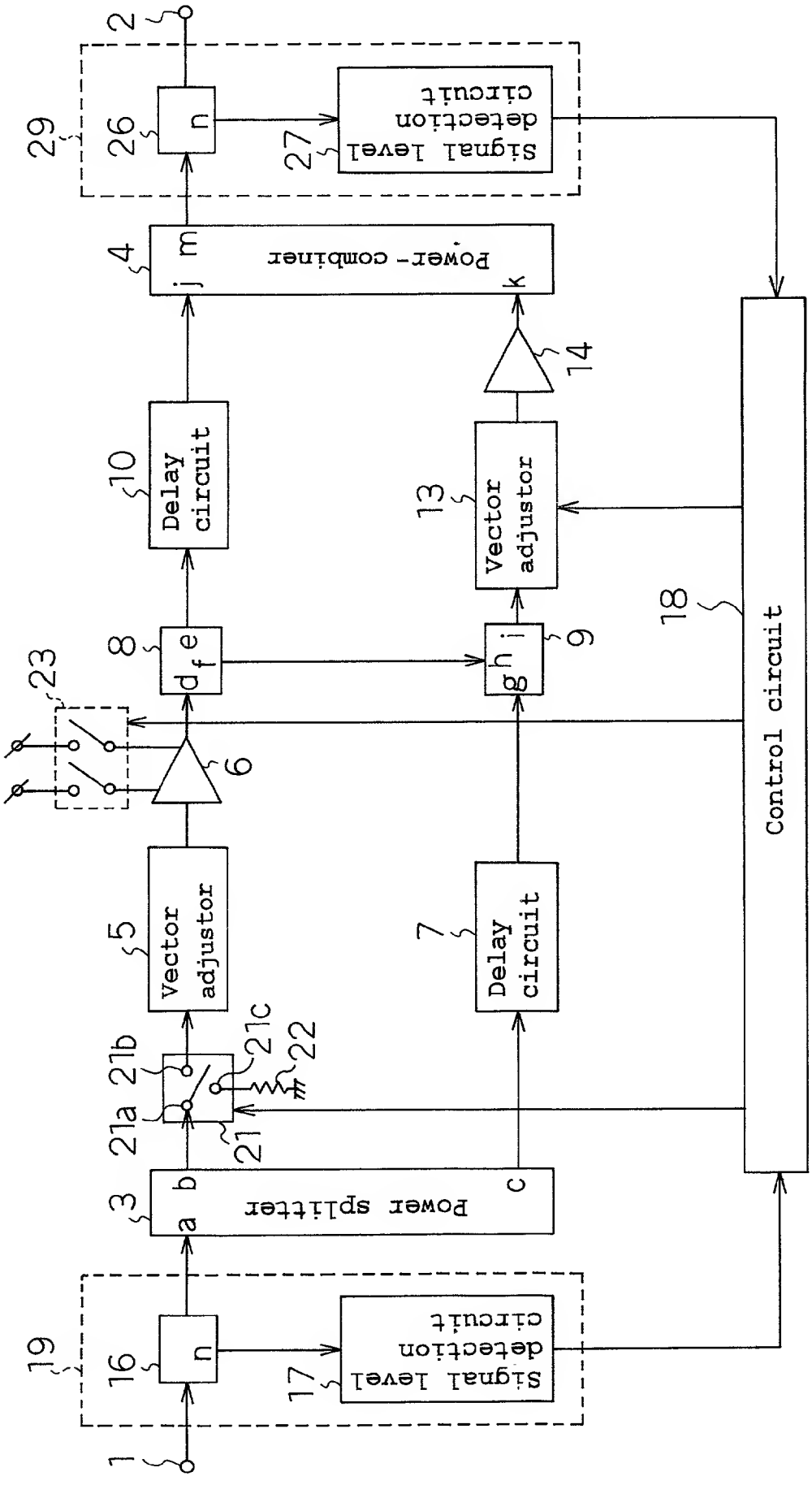


Fig. 3

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6
7
8
9
10
13
14
16
17
18
19
21
21a
21b
21c
22
23
26
27
29
n
Signal level detection circuit
Power splitter
Power-combiner
Vector adjustor
Delay circuit
Control circuit
a
b
c
d
e
f
g
h
i
j
k
m

Fig. 4

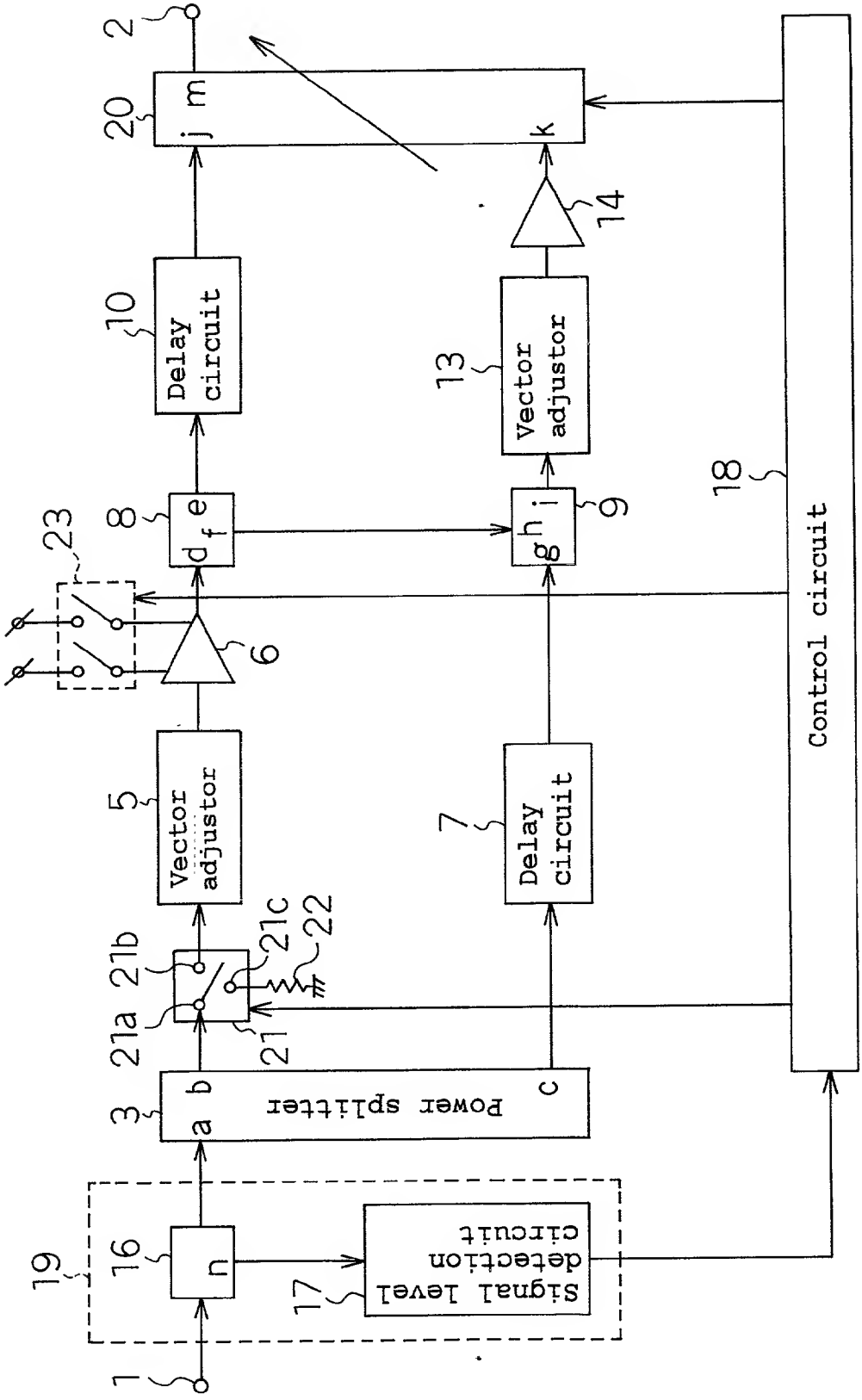
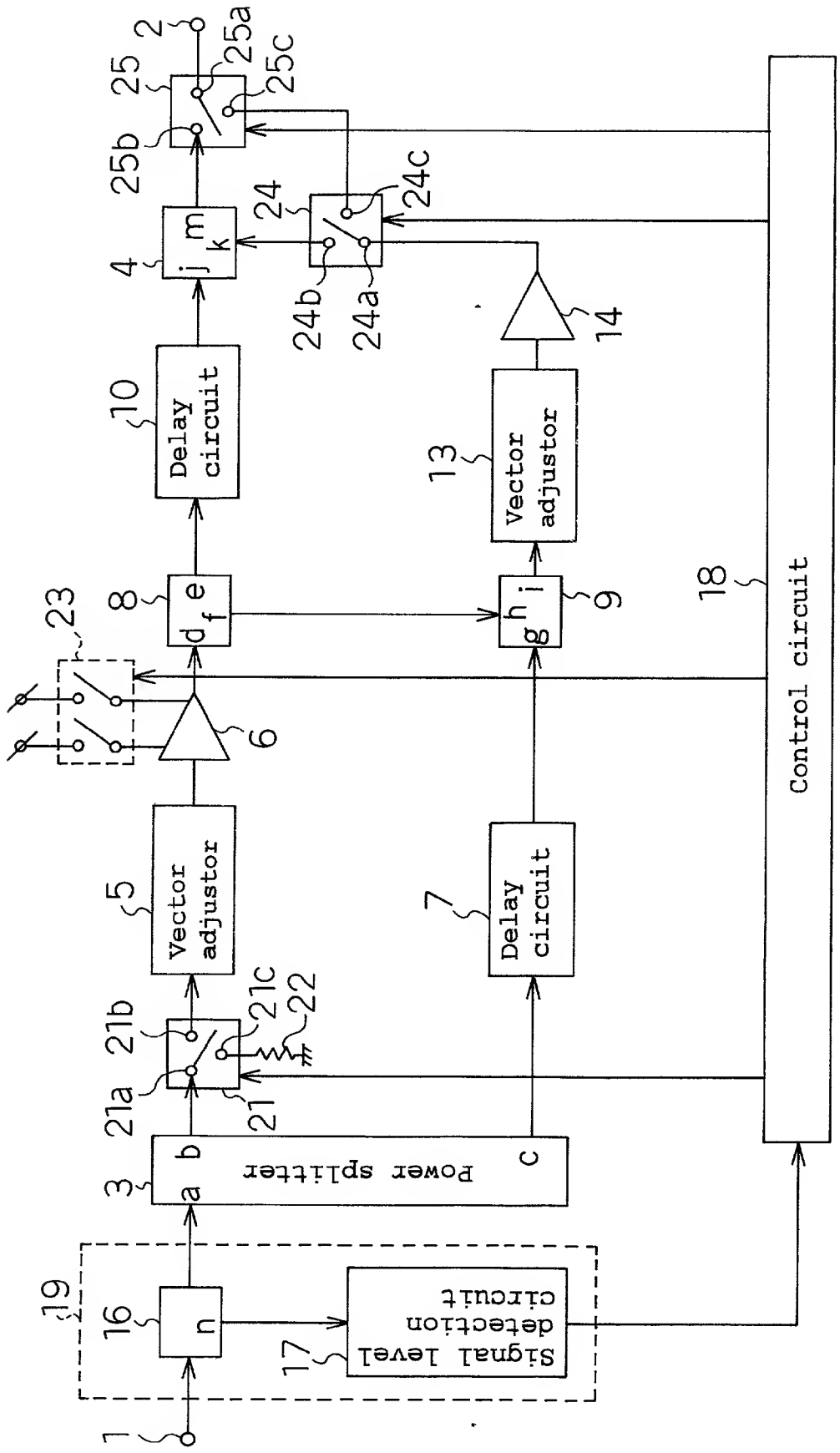

1
19
16
n
17
Signal level detection circuit
3
a
b
Power splitter
c
21a
21b
21c
22
21
5
Vector adjustor
7
Delay circuit
23
6
8
d
f
e
9
g
h
i
10
Delay circuit
13
Vector adjustor
14
20
j
m
k
2
18
Control circuit

Fig. 5

Fig. 6


1
2
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14
16
17
18
19
21
21a
21b
21c
22
23
24
24a
24b
24c
25
25a
25b
25c
n
Signal level detection circuit
a
b
c
Power splitter
Vector adjustor
Delay circuit
d
e
f
g
h
i
j
k
m
Control circuit

Fig. 7

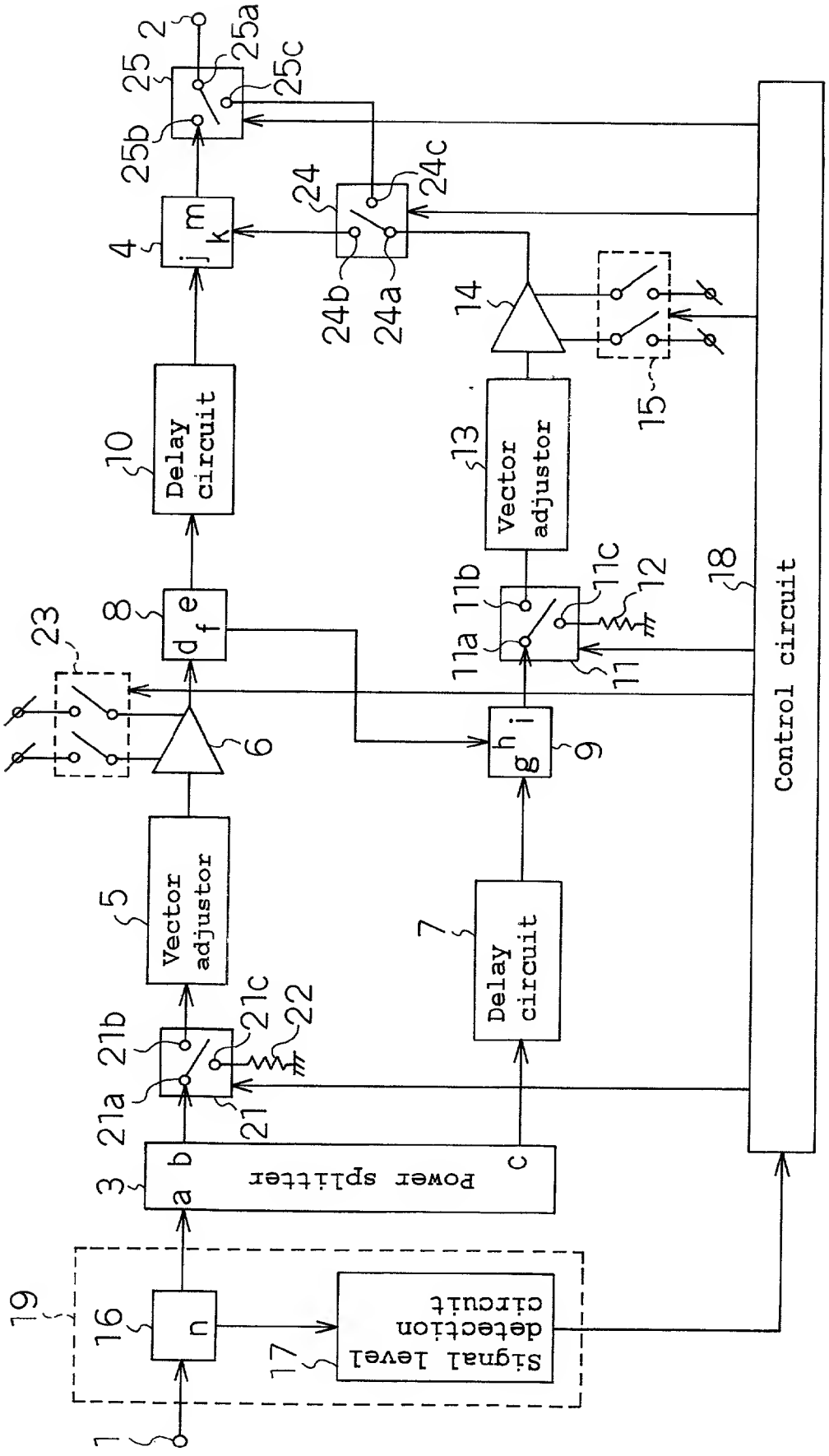
1
19
16
n
17
Signal level detection circuit
3
a
b
c
Power splitter
21a
21b
21c
21
22
5
Vector adjustor
7
Delay circuit
6
23
8
d
e
f
10
Delay circuit
4
j
m
k
25
25a
25b
25c
2
24
24a
24b
24c
14
15
13
Vector adjustor
9
g
h
i
11a
11b
11c
11
12
18
Control circuit

Fig. 8

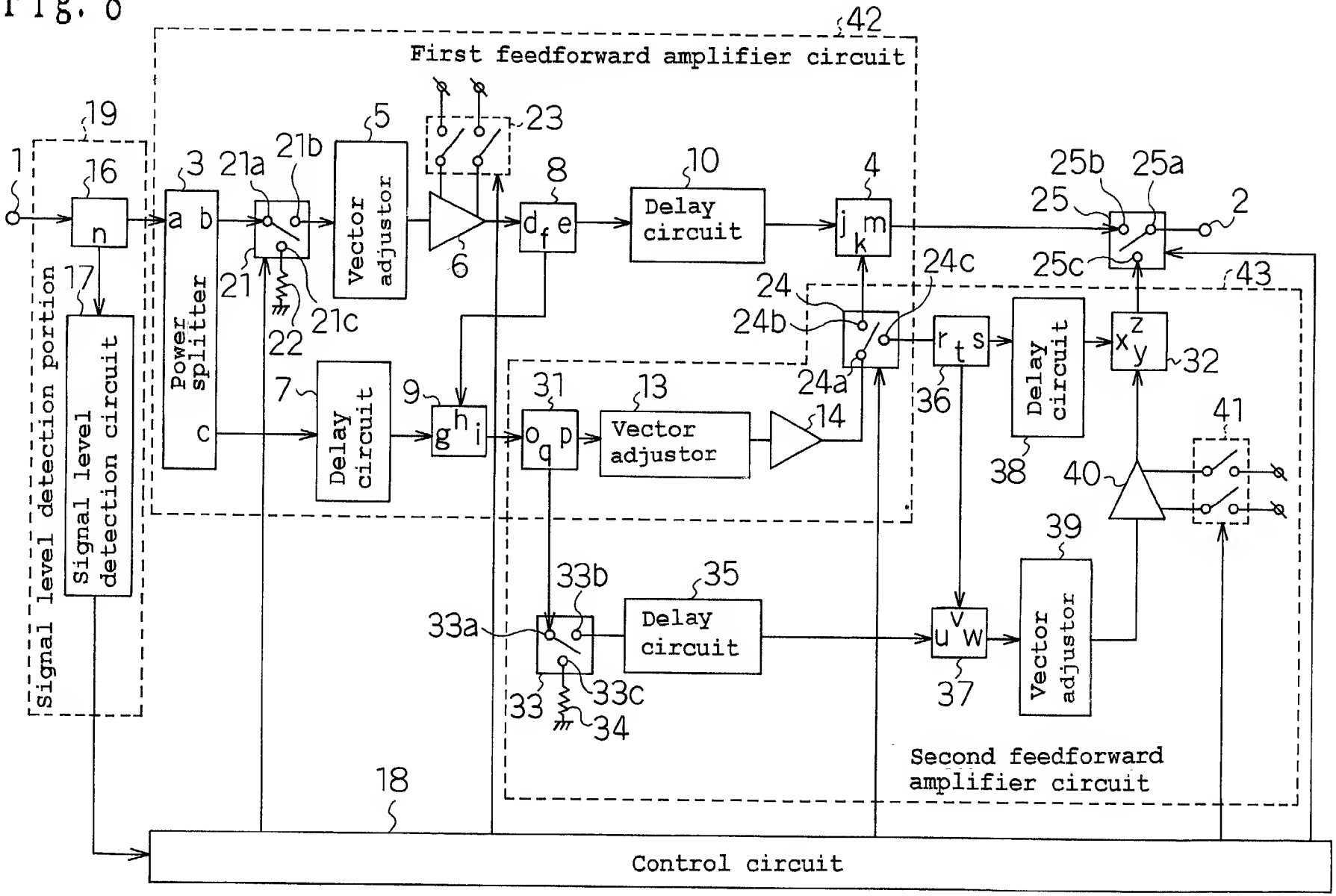
42
First feedforward amplifier circuit
19
1
16
n
17
Signal level detection circuit
Signal level detection portion
3
a b
c
Power splitter
21a
21b
21
22
21c
5
Vector adjustor
23
6
8
d f e
10
Delay circuit
4
j k m
25b
25a
25
2
25c
24c
24
24b
24a
43
r t s
36
Delay circuit
x z y
32
7
Delay circuit
9
g h i
31
o q p
13
Vector adjustor
14
38
40
41
39
33b
35
33a
Delay circuit
u v w
37
Vector adjustor
33
33c
34
Second feedforward amplifier circuit
18
Control circuit

Fig. 9

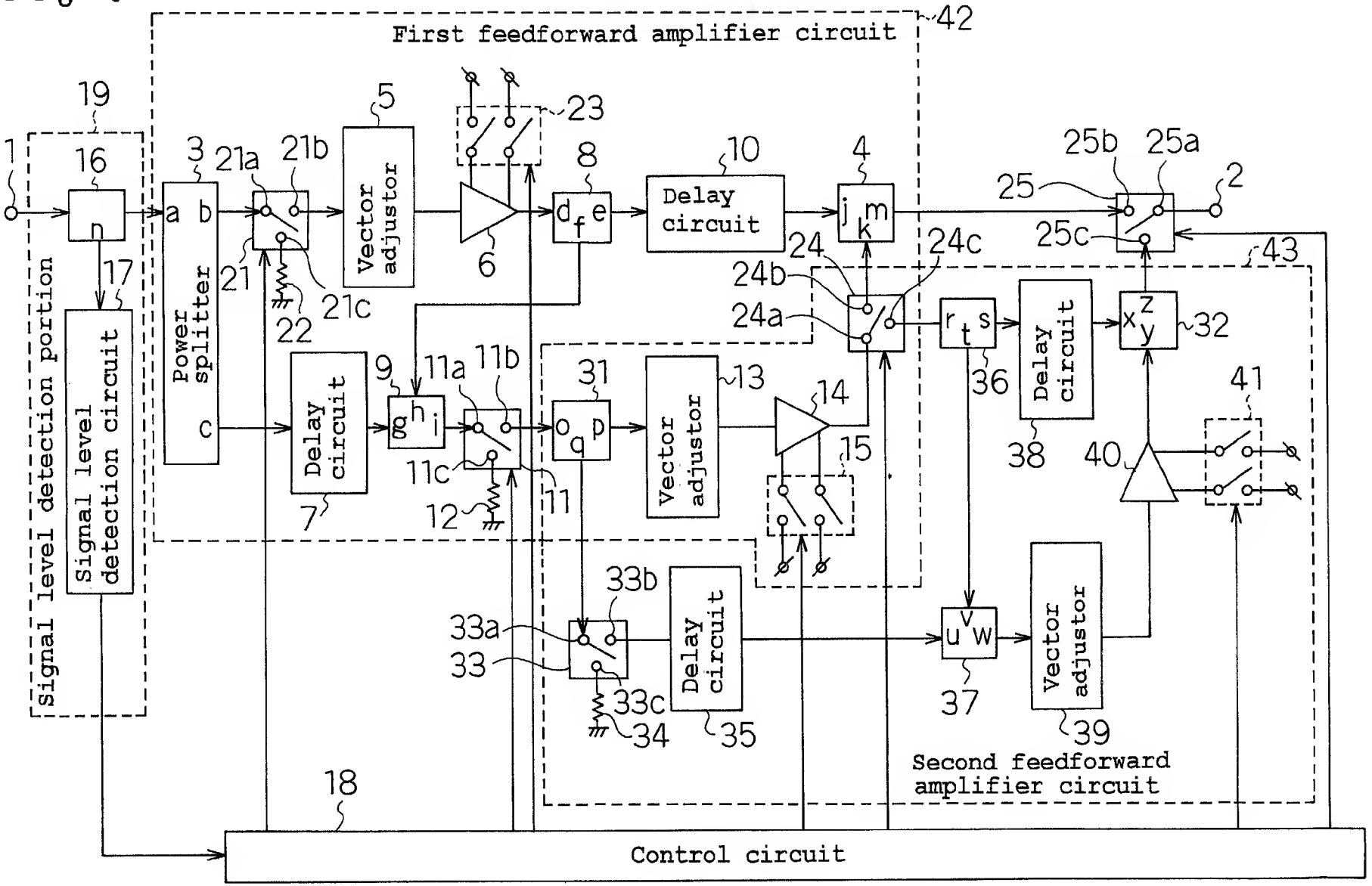
First feedforward amplifier circuit
42
Signal level detection portion
19
Signal level detection circuit
17
16
1
3
Power splitter
a
b
c
21a
21b
21
21c
22
Vector adjustor
5
23
6
8
d
f
e
Delay circuit
10
4
j
k
m
25
25b
25a
2
25c
24
24b
24a
24c
43
r
t
s
36
Delay circuit
38
x
y
z
32
41
40
Delay circuit
7
9
g
h
i
11a
11b
11c
11
12
31
o
q
p
Vector adjustor
13
14
15
33b
33a
33
33c
34
Delay circuit
35
u
v
w
37
Vector adjustor
39
Second feedforward amplifier circuit
18
Control circuit

Fig. 10

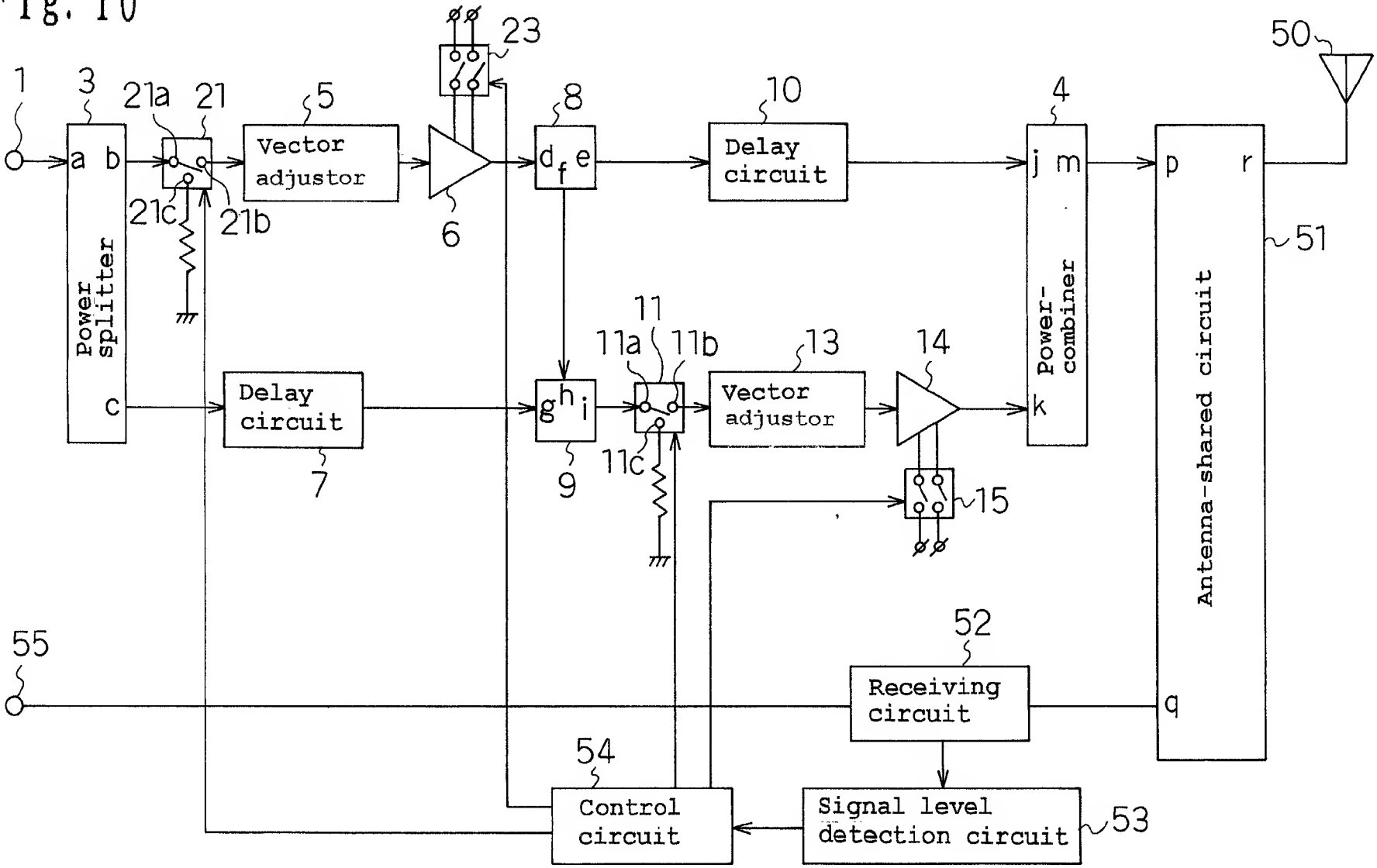
1
3
21a
21
5
23
8
10
4
50
a b
Vector adjustor
d f e
Delay circuit
j m
p r
21c
21b
6
Power splitter
Power-combiner
51
11
11a
11b
13
14
Antenna-shared circuit
c
Delay circuit
g h i
Vector adjustor
k
7
9
11c
15
55
52
Receiving circuit
q
54
Control circuit
Signal level detection circuit
53

Fig. 11

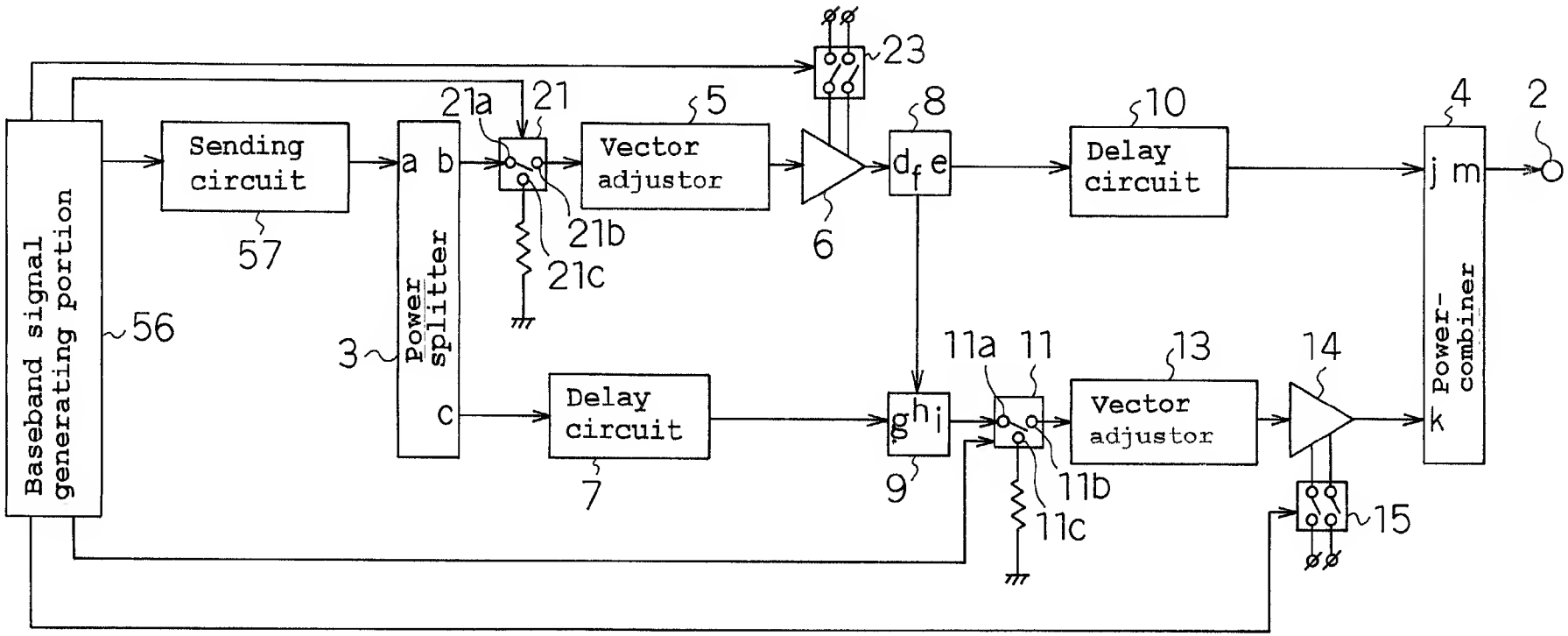
Baseband signal generating portion
56
Sending circuit
57
a b
c
Power splitter
3
21a
21
21b
21c
Vector adjustor
5
23
6
8
d f e
Delay circuit
7
g h i
9
11a
11
11b
11c
Vector adjustor
13
14
15
10
Delay circuit
4
j m
k Power-combiner
2

Fig. 12

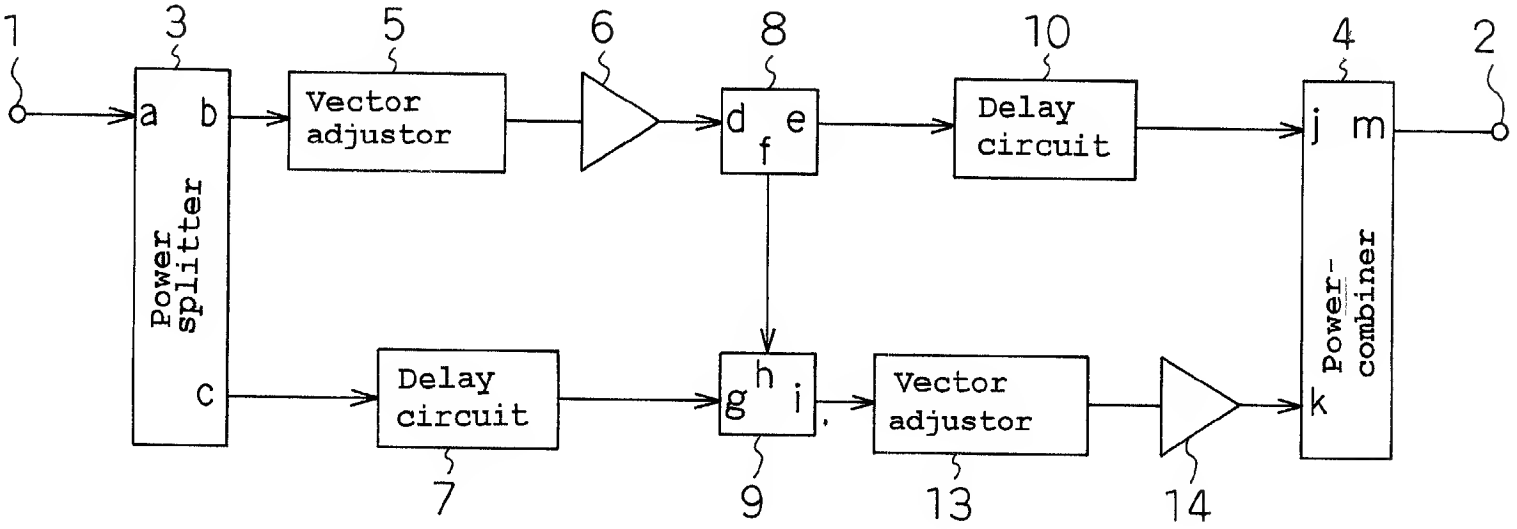
1
3
5
6
8
10
4
2
a
b
c
Power splitter
Vector adjustor
d
e
f
Delay circuit
j
m
k
Power-combiner
Delay circuit
g
h
i
Vector adjustor
7
9
13
14

Fig. 13 (a)

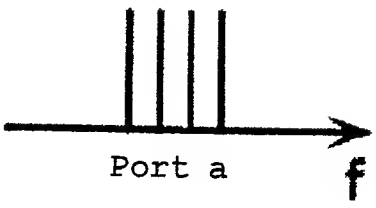

Fig. 13 (b)

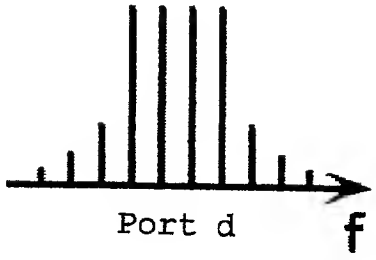

Fig. 13 (c)

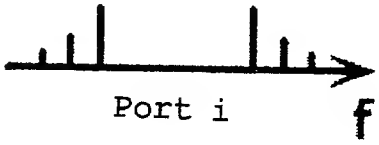

Fig. 13 (d)

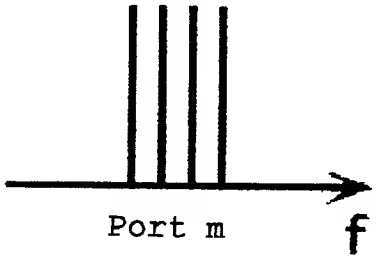

Fig. 14